74LV259

8-bit addressable latch

Product data sheet

1. General description

The 74LV259 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC259 and 74HCT259. The 74LV259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. The 74LV259 is multifunctional device capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q0 to Q7), functions are available. The 74LV259 also incorporates an active LOW common reset ($\overline{MR}$) for resetting all latches, as well as, an active LOW enable input ($\overline{LE}$).

The 74LV259 has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the (D) input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A0 to A2) and data (D) input. When operating the 74LV259 as an address latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode.

2. Features

- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical output ground bounce < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV259N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74LV259D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV259DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV259PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LV259BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

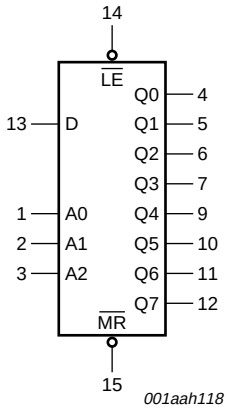


Fig 1. Logic symbol

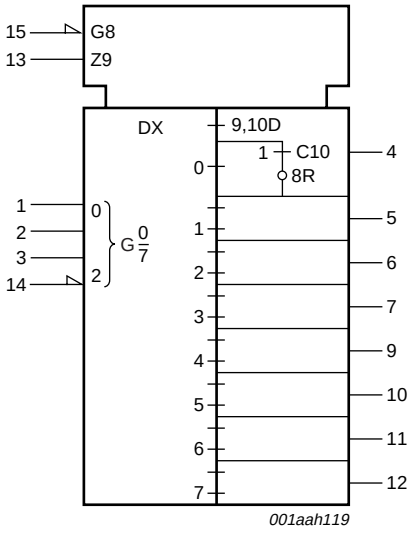


Fig 2. IEC logic symbol

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±50	mA
I_O	output current	$V_O = –0.5$ V to $(V_{CC} + 0.5$ V)		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = –40$ °C to +125 °C				
		DIP16 package	[2]	-	750	mW
		SO16 package	[3]	-	500	mW
		(T)SSOP16 package	[4]	-	500	mW
		DHVQFN16 package	[5]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	3.6	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature			–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V		-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V		-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V		-	-	100	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

9. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = –100 µA; V_{CC} = 1.2 V	-	1.2	-	-	-	V
		I_O = –100 µA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I_O = –100 µA; V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I_O = –100 µA; V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.2 V	-	0	-	-	-	V
		I_O = 100 µA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I_O = 100 µA; V_{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I_O = 100 µA; V_{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	-	1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20.0	-	160	µA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC}$ – 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	-	850	µA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; For test circuit see Figure 12.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	D to Qn; see Figure 8	[2]						
		V_{CC} = 1.2 V		-	105	-	-	-	ns
		V_{CC} = 2.0 V		-	36	49	-	61	ns
		V_{CC} = 2.7 V		-	26	36	-	45	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	17	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	20	29	-	36	ns
t_{pd}	propagation delay	An to Qn; see Figure 7	[2]						
		V_{CC} = 1.2 V		-	105	-	-	-	ns
		V_{CC} = 2.0 V		-	36	49	-	61	ns
		V_{CC} = 2.7 V		-	26	36	-	45	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	17	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	20	29	-	36	ns
t_{pd}	propagation delay	$\overline{LE}$ to Qn; Figure 6	[2]						
		V_{CC} = 1.2 V		-	100	-	-	-	ns
		V_{CC} = 2.0 V		-	34	48	-	60	ns
		V_{CC} = 2.7 V		-	25	35	-	44	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	16	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	19	28	-	35	ns
t_{PHL}	HIGH to LOW	$\overline{MR}$ to Qn; Figure 9							
	propagation delay	V_{CC} = 1.2 V		-	90	-	-	-	ns
		V_{CC} = 2.0 V		-	31	43	-	53	ns
		V_{CC} = 2.7 V		-	23	31	-	39	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	14	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	17	25	-	31	ns
t_W	pulse width	$\overline{LE}$, HIGH or LOW; see Figure 6							
		V_{CC} = 2.0 V		34	10	-	41	-	ns
		V_{CC} = 2.7 V		25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	20	6	-	24	-	ns
t_W	pulse width	$\overline{MR}$, LOW; see Figure 9							
		V_{CC} = 2.0 V		34	10	-	41	-	ns
		V_{CC} = 2.7 V		25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	20	6	-	24	-	ns

Table 8. Dynamic characteristics *...continued*

GND = 0 V; For test circuit see Figure 12.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{su}	set-up time	D, An to $\overline{LE}$; see Figure 10 and Figure 11							
		V_{CC} = 1.2 V		-	35	-	-	-	ns
		V_{CC} = 2.0 V		24	12	-	29	-	ns
		V_{CC} = 2.7 V		18	9	-	21	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	14	7	-	17	-	ns
t_h	hold time	D to $\overline{LE}$; see Figure 10							
		V_{CC} = 1.2 V		-	–30	-	-	-	ns
		V_{CC} = 2.0 V		5	–10	-	5	-	ns
		V_{CC} = 2.7 V		5	–8	-	5	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	5	–6	-	5	-	ns
t_h	hold time	An to $\overline{LE}$; see Figure 11							
		V_{CC} = 1.2 V		-	–20	-	-	-	ns
		V_{CC} = 2.0 V		5	–7	-	5	-	ns
		V_{CC} = 2.7 V		5	–5	-	5	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	5	–4	-	5	-	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[4]		19				pF

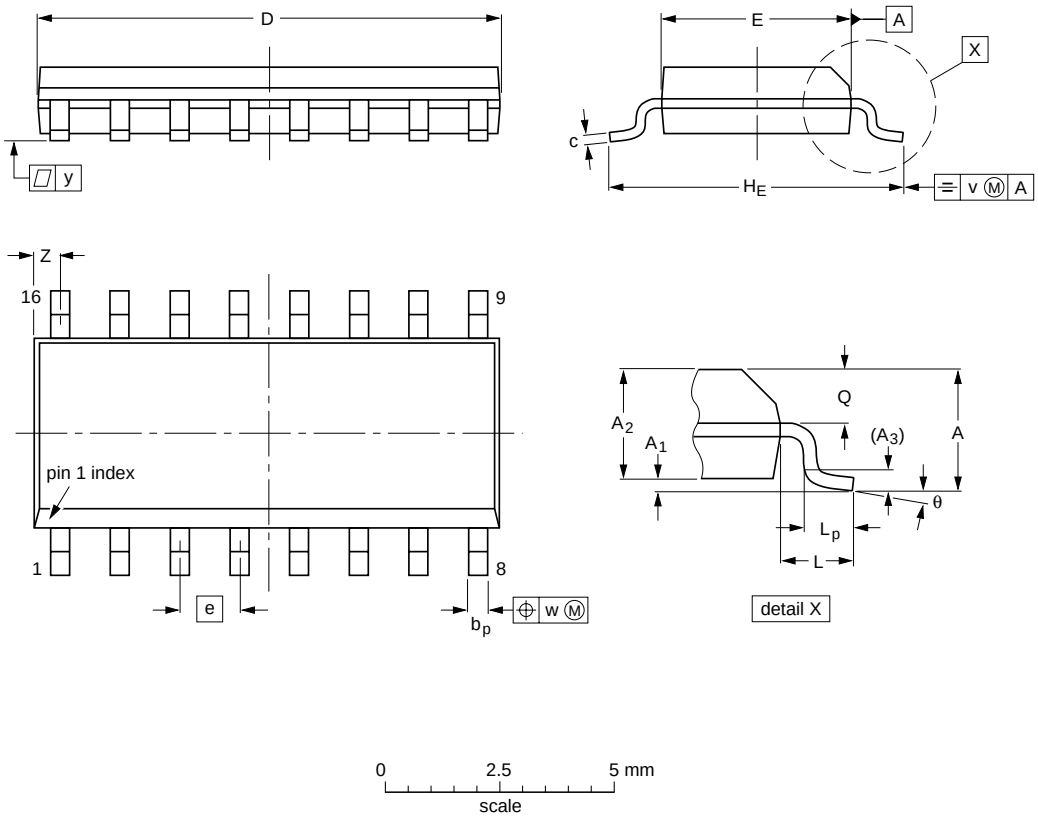
[1] Typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Typical value measured at V_{CC} = 3.3 V.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				

Fig 14. Package outline SOT109-1 (SO16)